devices. He joined Ain Shams University, Cairo, in 1968 first as a lecturer, then Assistant Professor and Professor. During this period he performed and supervised research and development of new microwave and millimeter-wave components and transmission media as well as providing consultation to several projects. Recent publications deal with the millimeter-wave performance of planar transmission lines including microstrip, fin and slot lines on isotropic and anisotropic substrates. Since March 1981 he is on a leave of absence from Ain Shams University, teaching engineering electromagnetics at University of California, Irvine, and persuing research.

Chip Level IMPATT Combining at 40 GHz

CHARLES T. RUCKER, SENIOR MEMBER, IEEE, JOHN W. AMOSS, SENIOR MEMBER, IEEE, AND GERALD N. HILL

Abstract—**Results with series and series–parallel connections of CW 40-GHz IMPATT diodes on diamond are discussed. The effects of device and circuit losses on the efficiency are treated. Device loss associated with the stabilizing capacitors appears likely as the major factor limiting the combining efficiency. Maximum combining efficiency of 82 percent has been demonstrated for two diodes connected in series. The multichip geometries utilize Raytheon gallium arsenide CW double-drift diode chips and are essentially scaled versions of successful *X*-band geometries previously reported [1] by the authors.**

I. Introduction

THE AUTHORS have reported successful work with series and series–parallel connected IMPATT devices at *X*-band frequencies [1]; it is desirable to extend this technique to millimeter frequencies if possible. Reported herein is work aimed at scaling the *X*-band multichip geometries and techniques to 40 GHz. Current results show the approach to be feasible with up to 82-percent combining efficiency; however, high combining efficiency (η_c) has not been routinely obtained. A possible explanation, related to capacitor loss, for some of the low η_c values is summarized. The effects of circuit losses are also treated. The function of the capacitors and criteria for their selection have been discussed in [1].

II. Geometry Fabrication

Fig. 1 is a sketch showing a typical successful *X*-band CW device and its nominally equivalent 40-GHz counterpart. The devices are not exactly to scale. Also shown, in Fig. 2, is an SEM photomicrograph of a typical two-chip 40-GHz device.

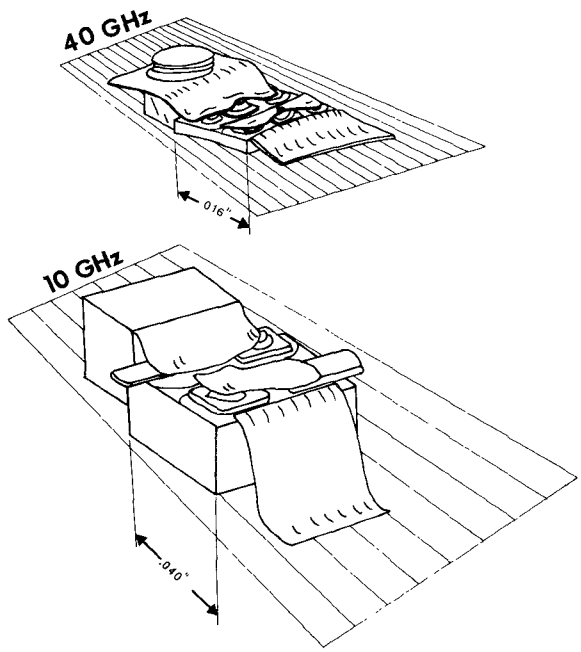


Fig. 1. Multichip IMPATT geometries, 10 GHz and 40 GHz.

In general, all dimensions, including diamond heat sink size, lead lengths, etc., have been held quite close to scale. The initial intent was to utilize diamond heatsinks between 0.010 and 0.013 in square for the 40-GHz work. This dimension was increased to 0.016 in in order to ease assembly problems and to accomodate diode and capacitor dimensions somewhat larger than anticipated. No identifiable spurious modes related to the increased size of the

Manuscript received April 13, 1981; revised August 10, 1981. This work was supported by the Avionics Laboratory, Air Force Wright Aeronautical Laboratory, Wright Patterson Air Force Base, OH.

The authors are with the Engineering Experiment Station, Georgia Institute of Technology, Atlanta, GA 30332.

0018-9480/81/1200-1266$00.75 ©1981 IEEE

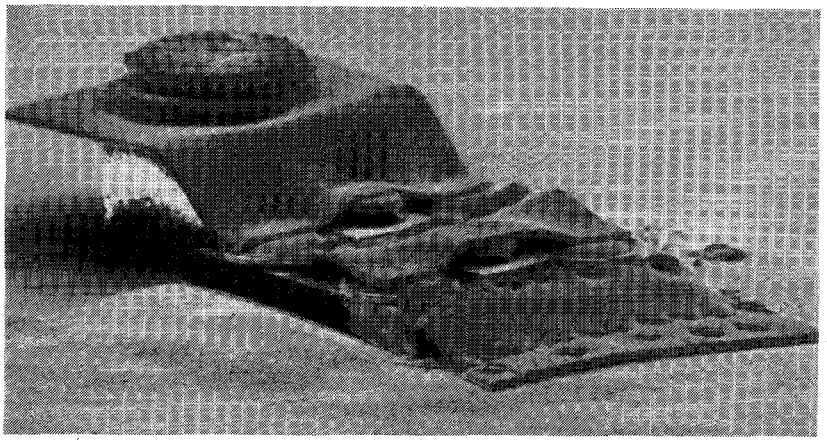


Fig. 2. SEM photomicrograph of 40-GHz geometry.

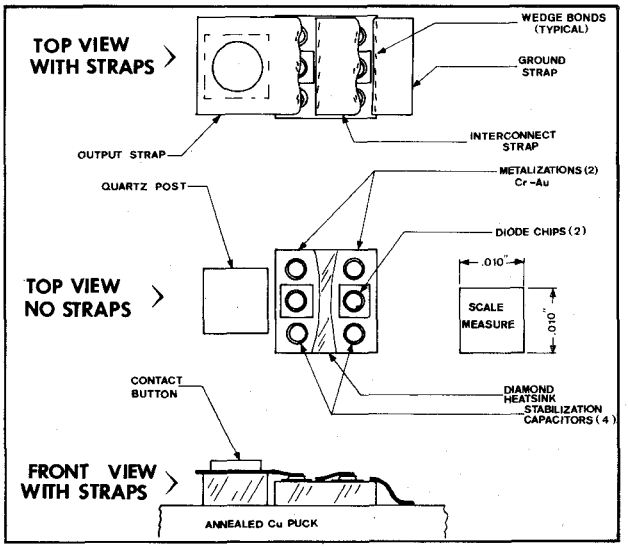


Fig. 3. Detailed sketch of 40-GHz multichip assembly.

geometry have been noted. On the other hand, certain unexplained anomalies noted in performance may imply the existence of such modes, especially in the case of three chip series devices.

Fig. 3 is a detailed sketch of a two-chip series-connected device (1×2) showing exact dimensions. This particular device provided the best combining efficiency noted (82 percent). Assembly was accomplished in the following manner.

1) T.C. bond diamond heatsink to 0.200-in diameter polished annealed (Knoop 50), Au-plated copper puck. The 0.005-in thick diamond is pressed 0.002–0.003 in into the puck surface ($P \approx 25$ kpsi, $T \approx 300$°C).

2) T.C. bond diode chips (2) in their respective locations ($P \approx 2$ kpsi, $T \approx 300$°C).

3) T.C. bond stabilization capacitors (4) in their respective locations ($P \approx 1.5$ kpsi, $T \approx 300$°C).

4) T.C. bond quartz post adjacent to diamond ($P \approx 1.5$–2.0 kpsi, $T \approx 300$°C). Puck surface adjacent to diamond is first pressed flat to remove deformation caused by T.C. bonding diamond (P = sufficient to flatten ≈ 20 kpsi, T = 300°C).

5) Wedge-bond foil-ground, interconnect, and output straps in that order ($T = 300$°C).

6) T.C. bond contact button ($P \approx 2$ kpsi, $T = 300$°C).

III. Results

Fig. 4 is a summary of significant electrical results to date. A number of packaged devices was tested to establish the nominal power and efficiency to be expected from the available Raytheon device lot. Power and efficiency of 0.8 W and 11.2 percent, respectively, were routinely achieved in a modified Kurokawa-type test fixture supplied by Raytheon. The fixture employs back short, integral E–H tuners and a choke-type bias filter followed by an absorber slug. The lower portion of Fig. 4 shows efficiency bounds noted during tests of numerous two-diode (1×2) series devices. Other multichip devices were also tested. The curve shown for the 2×2 device (two parallel pairs connected in series) is typical of the 1×2 as well as other multichip devices. In general, they all exhibit a well-behaved near-parallel set of curves between the bounds shown. An exception is the 1×3 (3 chips in series) device which shows a slight improvement over the best 1×2 at low input power

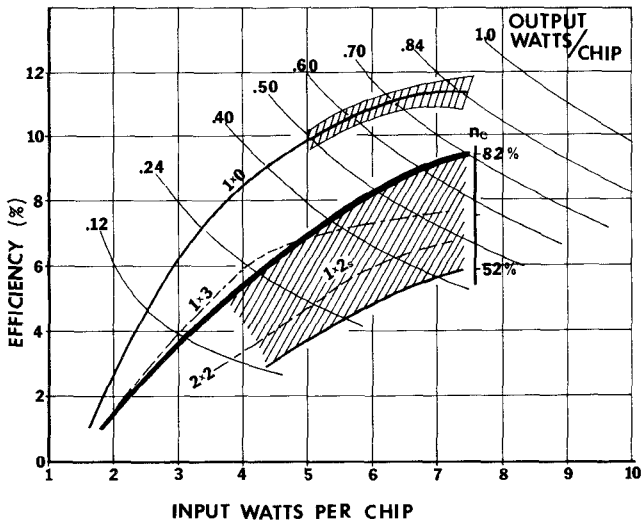


Fig. 4. Summary of measured RF performance with 40-GHz multichip geometries.

densities, but the efficiency degrades rapidly at higher inputs. Parametric effects were not noted and, thus far, we have not explained the sharp break in the 1×3 efficiency curve or established the preference of one geometry over another in terms of which may finally yield maximum efficiency.

IV. Efficiency Investigation

The percentage reduction in efficiency of the multichip devices is roughly independent of input power per chip, seeming to rule out nonlinear effects (parametric, mode jumping, etc.,) as a possible cause of the nominally low efficiency observed with many assemblies. The near-uniform reduction is thought to be more likely due to circuit or device loss. At the higher power levels, combining efficiency lying between 50–82 percent has been measured. Clearly, the 82-percent results are acceptable while values near 50 percent are useful only in rare cases. Several computer simulations of increasing complexity were devised to examine the effect of circuit and device loss on efficiency. For discussion purposes, all losses occurring outside the multichip device are considered circuit losses and those within are considered device losses. To obtain stable operation with series assemblies, it was necessary to use lumped SiO_2 capacitors in parallel with each diode chip in much the same manner as required for stability (with most devices) in X-band [1]. The losses associated with these capacitors and their connecting leads are considered as part of the device loss.

V. Circuit Loss

If fixed circuit loss (as opposed to fixed device loss/chip) is at fault, one would expect the efficiency to improve if the number of series connected devices is increased because of the increase in net negative resistance. This is illustrated in Fig. 5 for a hypothetical oscillator employing N series-connected active devices. Each chip is modeled as a 0.6-pF capacitor in series with a nonlinear negative resistor whose

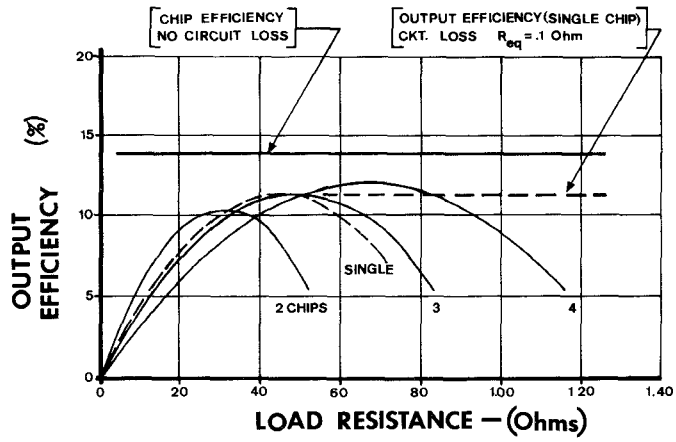


Fig. 5. Effect of circuit loss on multichip devices.

large-signal behavior is taken to be a quadratic function of RF current. To relate the model to a typical chip, the coefficients of the quadratic expression were chosen to give a small-signal resistance of $-1.0\ \Omega$ and a maximum output power of 0.8 W with a chip efficiency of 13.8 percent. These figures reflect the maximum efficiency and include loss occurring within the chip itself. This model yields an output efficiency of 11.2 percent for a single chip when operated in an oscillator circuit with an effective loss resistance of 0.1 Ω. This value and the -1.0-Ω small-signal chip resistance were estimated by circuit loss approximations and computer analysis of the test fixture. The latter is consistant with the -0.5-Ω large-signal chip resistance estimated by Raytheon.

An output efficiency curve calculated for a single-chip device without parallel capacitor is also shown in Fig. 5 (dashed curve). Maximum output power is obtained when the load resistance, transformed to the chip, is $R_L=(R_0-R_C)/2=0.45\ \Omega$, where R_0 is the magnitude of the small-signal chip resistance (1.0) Ω and R_C is the transformed circuit loss resistance (0.1 Ω). For the multichip devices, a lossless capacitance of 0.4 pF was shunted across each chip. Several general comments can be made based on these qualitative results. If fixed circuit losses predominate, the net effect of the lossless parallel capacitors in a 1×2 device is to lower the resistive part of the net impedance to a value lower than that for a single chip device without capacitor. For the assumed circuit loss of 0.1 Ω, the 1×2 chip device shows a lower calculated output efficiency than a single chip. It does, however, show a significantly higher value than that obtained experimentally, i.e., 91-percent combining efficiency versus 82–52 percent. It would require circuit loss resistances of between 0.20 and 0.43 Ω to reduce the efficiencies to this range, as illustrated in Fig. 6. We have been unable to justify such large circuit losses. Furthermore, we have not observed the dramatic increase in multichip efficiency which these losses would imply. The measured performance of multichip devices was in all cases inferior to that of single chip devices, contrary to expectations if large circuit loss existed. In short, the experimental data interpreted via the quadratic model (or other more subtle models) do not support the assumption that circuit loss combined with the reduced negative resistance due to

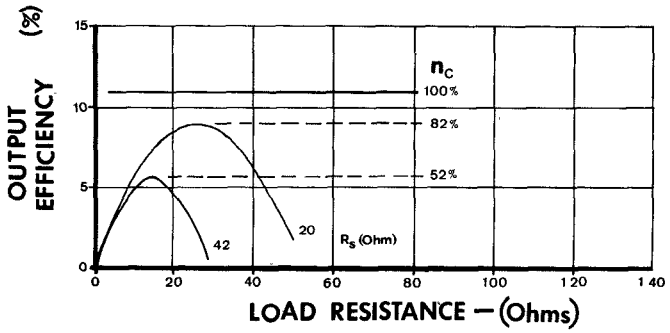


Fig. 6. Effect of higher circuit loss on multichip devices.

use of lossless stabilizing capacitors is at fault.

As stated previously, no multichip geometry could be shown experimentally to be consistently more efficient than another. This suggests that, if loss is responsible for the low combining efficiency, the loss per chip is approximately constant. The effect of loss in the multichip device itself, in particular that associated with the parallel capacitor, is examined next.

VI. Device Loss

Calculations similar to those just discussed were repeated assuming lossy stabilizing capacitors. The diode chip model was chosen this time to give an efficiency of 11.2 percent when operated in a lossless circuit. The range of Q values required to yield the observed range of efficiencies with the multichip-stabilized devices is shown in Fig. 7. Also shown, in Fig. 8, are representative plots of circuit Q for lumped and distributed elements as reported in Young and Sobol [2]. The parallel lines (Fig. 7) are computed based on the work of Sobol [3] and the measurements of DeBrecht [4]. At high microwave frequencies, lumped capacitor Q is almost totally controlled by conductor loss which is proportional to $C^{-1}(f)^{-3/2}$. The parallel lines shown are based on this relationship, and constants of proportionality determined from experimental data between 1 and 12 GHz. It should be noted that Q values measured at X-band are about six times lower than one would compute based on bulk properties of quartz with idealized metallizations and indicate loss mechanisms that are not fully understood. Some of the multichip devices tested used stabilizing capacitors made from thinly etched quartz while others used capacitors made from thermally grown SiO_2. No discernable difference in device operation was noted between the two types. The Q values required to decrease efficiency to 50 or 82 percent using our hypothetical model are in good agreement with the extrapolated values shown in Fig. 7.

A large signal diode model, based on the analysis of Statz, Pucel, Simpson, and Haus [5], was also used in these investigations. Their analysis is based on a "Read type model" in which the avalanche and drift regions are treated separately and later combined. Although certain high-power saturation effects cannot be included in this approach, it has been used successfully here and by others to model low and moderate power IMPATT's.

Initially, it was reasoned that if loss is, in fact, the major

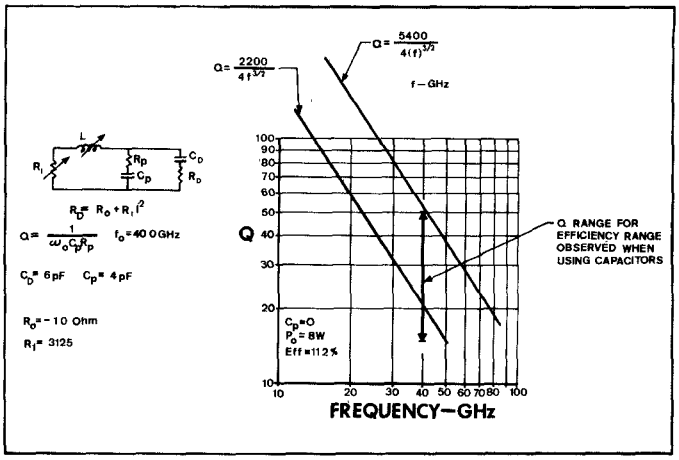


Fig. 7. Capacitor Q as a function of frequency.

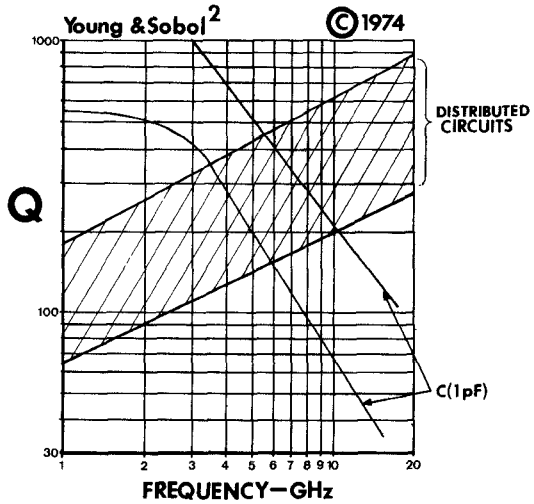


Fig. 8. Q of lumped elements as a function of frequency. (Young and Sobol [2]).

cause of poor multichip efficiency, then it should also cause the oscillation threshold of the stabilized devices to increase. In other words, the multichip devices should require significantly higher input power before the onset of oscillations than should single devices without stabilizing capacitors. The Statz model was modified to investigate the effects of circuit and device loss on oscillation threshold. The modification simulates the double-drift devices used by including another drift region. Most physical and material parameters used to characterize the avalanche region and both drift regions were estimated from Raytheon reports. The more nebulous parameters such as saturation current, intrinsic response time, etc., were adjusted to match the measured single chip efficiency. The results of these calculations, assuming lossy stabilizing capacitors are shown in Fig. 9.

These computed curves for the multichip devices are nearly perfect fits to the measured data of Fig. 4 for the range of capacitor Q values shown. These calculations, however, indicate that capacitor Q's as high as 125 significantly effect the efficiency, a result of the inability to include actual high-power saturation effects in this type model. The model, therefore, delivers maximum output power at a lower negative resistance than would actually

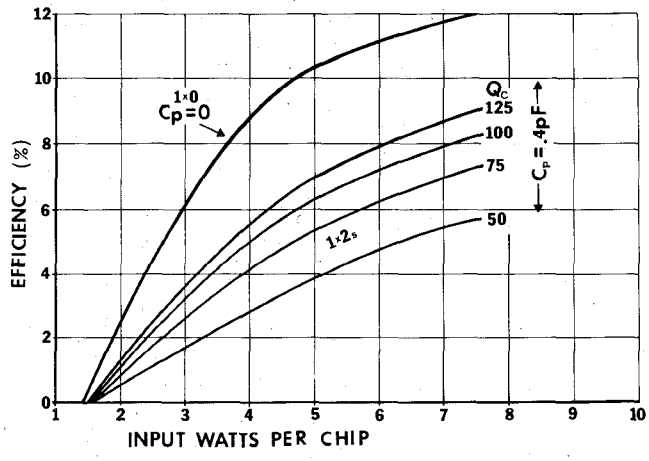


Fig. 9. Calculated large-signal RF performance for a range of capacitor Q's. Note agreement with measured performance of Fig. 4.

occur in practice and at a lower negative resistance than that assumed in the quadratic model.

The most important result of the calculations is that *circuit loss* in series with the chip(s) *should have a pronounced* effect on the threshold level while *capacitor loss* in parallel with each chip *should hardly effect* the threshold level. The close similarity of the calculated curves of Fig. 9 to the measured data of Fig. 4 provides additional support of the supposition that low capacitor Q coupled with lower devices impedance significantly degrades the output efficiency of 40-GHz multichip devices. Similar calculations at X-band, but scaling the respective Q's for the large-signal models, result in an X-band combining efficiency of 91 percent or better; values consistent with X-band performance previously reported.

VII. Conclusions

A scaling approach has resulted in stable 40-GHz multichip assemblies which do not appear to suffer from spurious modes related to physical geometry such as line length and parasitic effects. Maximum combining efficiency of 82 percent has been obtained but not routinely, possibly due to low Q of the stabilization capacitors.

Acknowledgment

The authors thank D. Masse and R. Bierig of Raytheon Semiconductor Research Laboratory for GaAs materials and device chips. The contributions and assistance of Lt. D. Allen, AADM-2, Avionics Laboratory AFWAL are also acknowledged.

References

[1] C. T. Rucker, J. W. Amoss, G. N. Hill, and N. W. Cox, "Multichip IMPATT power combining, a summary with new analytical and experimental results," *IEEE Trans. Microwave Theory Tech.*, vol, MTT-27, pp 951–957, Dec. 1979.

[2] L. Young and H. Sobol, *Advances in Microwaves*. New York: Academic, 1974, p. 196.

[3] ——, *Advances in Microwaves*. New York: Academic, 1974, p. 163.

[4] R. E. DeBrecht, "Impedance measurements of microwave lumped-elements from 1 to 12 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-20, pp. 41–48, Jan. 1972.

[5] Statz, Pucel, Simpson, and Haus, "Noise in gallium arsenide avalanche read diodes," *IEEE Trans. Electron Devices*, vol, ED-23, pp. 1075–1085, Sept. 1976.

Charles T. Rucker (S'56–M'69–SM'79) was born in Augusta, GA, on June 30, 1931. He received the B.E.E. degree from Georgia Institute of Technology, Atlanta, in 1957 and has completed additional work in mathematics and microwaves through the University of Florida, Gainesville.

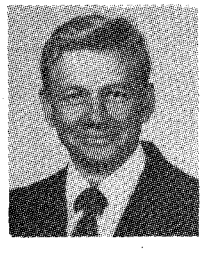
From 1957 to 1971 he was employed by the Sperry Microwave Electronics Division of Sperry Rand where he progressed to the level of Engineering Staff Consultant. His responsibilities during this period included development of ferrite components, parametric amplifiers, semiconductor switching components and solid-state signal sources and amplifiers. In 1971 he transferred to the Sperry Electronic Tube Division of Sperry Rand where he continued work on various active solid-state devices including Gunn, BARITT, and TRAPATT, and on unique power combining techniques for such devices. In 1973 he joined the staff of the Engineering Experiment Station, Georgia Institute of Technology, Atlanta, where he is presently a Senior Research Engineer in the Physical Sciences Division of the Electromagnetics Laboratory. His duties presently include responsibilities for various microwave solid-state research tasks with emphasis on power combining at the device-chip level. He has four patents granted or pending and has authored or co-authored numerous papers and reports in the area of microwave solid-state circuits.

Mr. Rucker is a member of Eta Kappa Nu, and has served as program committee co-vice chairman and as Guest Editor for the December 1974 IEEE TRANSACTIONS ON *Microwave Theory and Techniques*. He is serving a second term on the MTT-S Administrative Committee and is presently Operations Committee Chairman.

John W. Amoss (M'65–SM'70) was born in Fairburn, GA, in 1933. He received the B.E.E. degree from Auburn University, Auburn, AL, in 1955, the M.S.E.E. degree from the Georgia Institute of Technology, Atlanta, GA, in 1958, and the Ph.D. degree in electrical engineering from Auburn University in 1972.

In 1958 he joined Sperry Microwave Electronics Division, Sperry Rand Corporation, Clearwater, FL, where he was a Senior Member of the Research Staff. His work at Sperry was in the areas of parametric devices, tunnel-diode amplifiers, low-noise-figure measurement techniques, microwave properties of ferroelectric materials and devices, and direct power generation. In 1972, he joined the Physical Sciences Division of the Engineering Experiment Station, Georgia Institute of Technology, Atlanta, as a Senior Research Engineer where he has been active in research on microwave solid-state devices.

Dr. Amoss is a member of Eta Kappa Nu, Pi Mi Epsilon, and Sigma Xi.



Gerald N. Hill was born in Ironwood, MI, on December 7, 1935. He joined the United States Air Force in January 1955 and graduated from the radar electronics school at Keesler Air Force Base, Biloxi, Missouri. After his discharge he attended St. Petersburg Junior College, St. Petersburg, FL.

From 1958 to 1971 he was employed by the Sperry Microwave Electronics Company in Clearwater, FL. He progressed to the level of associate engineer and was responsible for devel-

opment and production of active solid-state devices in support of "in-house" requirements. Such devices included IMPATT and TRAPATT diodes, silicon and GaAs mixers, and Gunn, varactor, and p-i-n diodes. In 1971 he transferred to the Sperry Electronic Tube Division where he continued semiconductor device work with emphasis on chip level power combining techniques. In 1974 he joined the staff of the Engineering Experiment Station, Georgia Institute of Technology, Atlanta, where he is presently a Research Engineer in the Physical Sciences Division of the Electromagnetics Laboratory. He is heavily involved with both chip level power combining of CW and pulsed IMPATT devices and beam lead gallium arsenide mixer diodes. He is co-author of several papers in the area of microwave solid-state research.

The Effects of High Power Microwave Pulses on Red Blood Cells and the Relationship to Transmembrane Thermal Gradients

ALBERT W. FRIEND, JR., MEMBER, IEEE, SUSAN L. GARTNER, KENNETH R. FOSTER, MEMBER, IEEE, AND HARLAN HOWE, JR., FELLOW, IEEE

Abstract—**Calculations based on an idealized spherical model show that the relaxation times of transmembrane thermal gradients in red blood cells, and cells in general, are much less than 1 μs. Heat cannot be stored across the membrane during microwave pulses and only intense pulses can cause substantial transmembrane temperature gradients. Experiments show no hemolysis in red blood cells exposed *in vitro* to large microwave pulses with peak SAR's of more than 1 kW/g.**

List of Symbols

Λ_s Complex electrical conductivity of suspension.
Λ_A Complex electrical conductivity of medium.
Y Complex electrical conductivity of cytoplasm.
p Volume fraction of cells (hematocrit).
σ Electrical conductivity.
ϵ_0 Permittivity of space.
ϵ Relative dielectric constant.
ω $2\pi f$ (angular frequency).
f frequency.
ΔT Temperature drop across membrane.
V Volume of cytoplasm.
h Thermal conductance per unit area of membrane.
γ Fractional difference in power absorption.
P Specific absorption rate (SAR) during peak of pulse.
A Area of cell membrane.
θ Temperature displacement.
θ_0 Temperature displacement at time zero.
r Radial position.
R Radius of cell.
a k/C.
k Thermal conductivity of cytoplasm.
C Thermal capacitance of cytoplasm.
h Thermal conductance per unit of cell membrane.
t Time.

Manuscript received April 13, 1981; revised August 4, 1981. This work was supported by the Naval Medical Research and Development Command, NNMC, Department of the Navy, under Research Task No. MRO41.08.01.0109, and by Microwave Associates, Burlington, MA. The opinions and assertations contained herein are the private ones of the authors, and not to be construed as official or as reflecting the views of the Navy Department or the Naval Department at large.

A. W. Friend is with Naval Electronic Systems Command, Washington, DC 20360.

S. L. Gartner is with Naval Medical Research Institute, Bethesda, MD 20014.

K. R. Foster is with the Department of Bioengineering, University of Pennsylvania, Philadelphia, PA 19104.

H. Howe, Jr., is with Microwave Associates, Inc., Burlington, MA 01803.

I. Introduction

THE ELECTRICAL conductivities of the cytoplasm and extracellular fluids of biological cells are similar at microwave frequencies but not identical. The temperature differences created across the cell membrane due to differential absorption of continuous wave (CW) microwave radiation in the cytoplasm and extracellular fluids are extremely small, as we shall show. Pulsed microwaves with the same average power can create larger transient temperature differences. We calculate here the magnitude of these transients. Particular attention will be paid to red blood cells, since we have studied hemolysis during exposure to pulses at 2450 MHz in a microstrip exposure system [1]. The conclusions, however, are generally applicable to other kinds of cells.

The red cell study was motivated by predictions that small transmembrane temperature differences could cause

0018-9480/81/1200-1271$00.75 ©1981 IEEE